L Number	Hits	Search Text	DB	Time stamp
-	362747	Integrated adj Circuit	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/16 13:57
-	10	((Integrated adj Circuit) and (PLD or "Programmable Logic")) and configur$4 near (database or "data base" DBMS OODB DB)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/16 14:09
-	67770	(word or bit) near line	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/19 10:37
-	5723	(((word or bit) near line) and cell) and instance	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/19 10:38
-	300	(((word or bit) near line) and cell) and (logical same (name id))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/19 10:41
-	51	(((word or bit) near line) and cell) and (((((word or bit) near line) and cell) and instance) and (instance same path)) and ((((word or bit) near line) and cell) and (logical same (name id)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/19 14:41
-	249	cadence and hierarch$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/19 14:42
-	26	707/100 and (Logic adj device)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/19 15:15
-	46	(327/37-39.ccls. and instance) not (327/37-39.ccls. and address)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/19 15:30
-	15	(CADENCE.AS. and config$5) and address	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/19 15:35
-	578	((((memory near cell) and (PLD or logic)) and (bit with order$4)) and configur$5) and (identify same address)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/19 16:05
-	19	(((((memory near cell) and (PLD or logic)) and (bit with order$4)) and configur$5) and (identify same address)) and (load$4 near device)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/19 16:19
-	216	FPGA and (bit near order)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/19 16:50
-	162	(FPGA and (bit near order)) and configur$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/20 07:27

-	97	((((((configuration same block) and schema$4) and programmable same (device array)) and hierarch$4) and address) and (memory same cell)) and simulat$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/20 08:22
-	1032	((stor$4 load$4) and order and configur$4) and ("logical unit")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/27 10:55
-	62	load$4 near (device unit) same configur$4 same (programmable CPLD PLD FPGA Array)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/27 11:08
-	46	(loading with (programm$4 near6 (device array) PLD) same (order sequence)) and address	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/03 09:26
-	163	(wordline and location) and ((((wordline and location) and (X Y)) and bitline) and wordline same (X Y))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/03 16:27
-	21	(((wordline and location) and (X Y)) and bitline) and wordline near (X Y)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/03 16:28